REMARKS

Claims 1-22 and 53, as amended, and new claim 59 are before the Examiner for consideration. Claims 23-52 and 54-58 have been cancelled to advance prosecution.

Applicants appreciate the statements in the Office Action that claims 8 and 19 would be allowable if rewritten in independent form to include all of the limitations of the independent claim from which it depends; claims 8 and 19 have been so amended. New claim 59 depending from claim 9 recites a fault detecting method wherein the past use includes a number of past operations, a number of past defects, a reliability test status, and a number of process achievements. See applicants' specification, page 29, first two paragraphs for support of the subject matter of the new claim.

1. In response to the restriction requirement stated in the Office Action mailed November 29, 2004, applicants hereby provisionally elect Group I, claims 1-22 and 53 (and new claim 59). The non-elected claims have been cancelled to advance prosecution. Applicants will rely on the protection afforded by

35 U.S.C. §121 regarding any divisional application that may be filed.

2. Claims 54-58 were rejected under 35 U.S.C. §112, first and second paragraphs, as allegedly being indefinite and failing to comply with the enablement requirement, and rejected under 35 U.S.C. §101 as directed to allegedly non-statutory subject matter. The claims are cancelled; the rejections are moot.

3. Claims 1 and 3 were rejected under 35 U.S.C. §102(e) over Balachandran U.S. Patent 6,618,830. The claims patentably define thereon.

The fault detecting method of claim 1 includes providing a fault list corresponding to (a) information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, and (b) information required to reduce faults; and detecting faults in accordance with said fault list in a semiconductor integrated circuit to which said fault list corresponds. This method is nowhere disclosed or suggested in the cited reference.

Balachandran '830 is said to disclose a stuck-at-fault directory that allegedly corresponds to applicants' fault list. However, the reference at column 3, lines 56-57, and Fig. 2, explains that the document does not disclose a stuck-at-fault directory including physical layout information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, as recited in applicants' claim 1.

Claim 3, which depends from claim 1, is allowable for the same reasons explained herein for claim 1. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

4. Claims 2, 4-6, 9, 12-17, 20 and 53 were rejected under 35 U.S.C. §103(a) over Balachandran '830 in view of Rohrbaugh, et al. U.S. Patent 6,067,651; claims 7 and 18 were rejected under 35 U.S.C. §103(a) over Balachandran '830 and Rohrbaugh '651 in view of Allan U.S. Patent 6,066,179; and claims 10, 11, 21 and 22 were rejected under 35 U.S.C. §103(a) over Balachandran '830

and Rohrbaugh '651 in view of Agrawal et al. U.S. Patent 5,257,268. All rejections are respectfully traversed.

In the first instance, claims 2 and 4-7, 9-11 and 53, which depend directly or indirectly from claim 1, are allowable for the same reasons that claim 1 is allowable.

Moreover, regarding claim 5, Balachandran '830, column 9, line 51 to column 10, line 2, and Fig. 3, discloses a "defect size distribution" which represents a ranked list of faults and probability of occurrence of a defect of a particular size. The "defect size distribution" is used, however, to determine if such distribution could cause physically bridging faults, a determination different from the use of weighting of faults called for in the presently claimed invention. Balachandran '830 does not disclose weighting. The weighting of the presently claimed invention is to obtain fault coverage as accurately as possible by taking into account actually occurring faults. This weighing is to determine an accurate relationship between a defect level in the market and the fault coverage (see applicants' equation 1 on page 15), which leads to a reduction in the defect level in the market.

The difference between the Balachandran '830 technique and the presently claimed invention is shown below. According to Balachandran '830, it is "impossible" to obtain fault coverage from a fault list, whereas the presently claimed invention makes it possible to obtain fault coverage by means of weighting, as the examples below show:

Present Invention

| Fault List | Weighting | Fault Coverage |
|---|---|---|
| Fault 1 | 25.3 | 25.3 |
| Fault 2 | 14.2 | 39.3 |
| Fault 3 | 14.1 | 53.6 |
| Fault 4 | 13.9 | 67.5 |
| Fault 5 | 2.7 | 70.2 |

Balachandran '830

| Fault List | Weighting | Fault Coverage |
|---|---|---|
| Fault 1 | 1 | ? |
| Fault 2 | 2 | ? |
| Fault 3 | 3 | ? |
| Fault 4 | 4 | ? |
| Fault 5 | 5 | ? |

According to Balachandran '830, fault coverage cannot be known even if specifics in the fault list are detected.

Regarding claim 9, the Examiner asserts that Balachandran '830 discloses that "detecting defects" themselves includes the step of using functional blocks for detecting faults of the functional blocks. Claim 9, in contrast, recites "records of past use," which includes not only data obtained by using cells or functional blocks of a semiconductor integrated circuit and detecting reliability of such data, but also the number of past uses, the number of past defects, the state in the reliability test, and the number of successful processes as shown by applicants' seventh embodiment and Fig. 17.

Balachandran '830 does not disclose or suggest considering reliability data based on records of past use of cells or functional blocks of a semiconductor integrated circuit to which the fault list corresponds, and determining likelihoods of occurrence of defects based on the reliability data, as recited in applicants' claim 9.

As to claim 12, Balachandran '830 is alleged to disclose a stuck-at-fault directory corresponding to applicants' fault list. However, Balachandran '830, column 3, lines 56-57, and Fig. 2, as explained above, does not disclose or suggest a stuck-at-fault directory including physical layout information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur. Accordingly, Balachandran '830 does not disclose or suggest combining the detection result with (a) information about physical sites on a physical layout of the semiconductor integrated circuit to which said fault list corresponds where a possible fault is likely to occur and (b) information required to reduce faults, to create a fault list; and again detecting faults according to the fault list in such semiconductor integrated circuit, as recited in applicants' claim 12. The rejections should be withdrawn.

All claims 1-22, 53 and 59 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 1-22, 53 and 59 is respectfully requested.

The Examiner is informed that an Information Disclosure Statement was timely filed December 14, 2004. The Examiner is requested to consider that document along with the present paper.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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